

REMARKS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 1-23 are presently active in this case, Claim 11 having been amended and Claims 21-23 having been added by way of the present Amendment. Claims 2-4, 7, 8, 10, 11, 14, 16, 17, and 20 have been indicated as containing allowable subject matter.

Care has been taken such that no new matter has been entered by the amendment set forth herein, which are fully supported by the original disclosure of the present invention.

The Applicant notes that the Official Action was never received by the Applicant or the Applicant's representative. The issuance of the Official Action was discovered on June 2, 2005, as was discussed in detail in the Request to Reset the Reply Period filed by the Applicant on June 8, 2005. Additionally, it is noted that the public PAIR system clearly indicates that the Official Action was returned to the U.S. Patent and Trademark Office as being undelivered (despite the correct listing of the Applicant's representative's contact address in the Patent Office records), and no further attempts were made to ensure that the Applicant received a copy of the Official Action in a timely manner. Since the Applicant has not received any response to the Request filed on June 8, 2005, and since the six month period of time for response ends on July 21, 2005, the Applicant is filing a three month extension of time along with the present response to prevent the application from going abandoned. However, the Applicant respectfully requests that this issue be address by

resetting the period for response (which affects issues such as patent term extension calculations) and not requiring the payment of extensions of time in the present instance.

In the outstanding Official Action, Claims 1, 5, 6, 9, 12, 13, 15, 18, and 19 were rejected under 35 U.S.C. 103(a) as being unpatentable over Morioka et al. (U.S. Patent No. 5,274,434) in view of Chen et al. (U.S. Patent No. 5,726,920). For the reasons discussed below, the Applicant traverses the obviousness rejection.

The basic requirements for establishing a *prima facie* case of obviousness as set forth in MPEP 2143 include (1) there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings, (2) there must be a reasonable expectation of success, and (3) the reference (or references when combined) must teach or suggest all of the claim limitations. The Applicant submits that a *prima facie* case of obviousness has not been established in the present case because the cited references, either when taken singularly or in combination, do not teach or suggest all of the claim limitations.

Before addressing the specific distinction between the claimed invention and the cited references, a brief description of the background of the invention will be given.

In general, plural manufacturing apparatuses are often used in parallel in a manufacturing process in a production line of semiconductor devices. When the yield of lots processed by a manufacturing apparatus from among the plurality of manufacturing apparatuses is lower than those of the other manufacturing apparatuses, there is a possibility that the cause of the lower yield is inherent to the manufacturing apparatus. Therefore, in

order to improve the yields of the manufacturing apparatuses, it is required that the failing manufacturing apparatus be detected early in order to analyze the cause of the lower yield.

In the related art, differences in yield distributions between manufacturing apparatuses are usually analyzed without considering time axes in detecting a failing manufacturing apparatus.

However, when the plural manufacturing apparatuses are used unevenly in terms of time, analyzing only the differences of the yield distributions without considering the time axes may lower the capability to detect failing manufacturing apparatuses and produce false reports. Furthermore, when the number of target lots is increased in order to reduce false reports in number and raise the capability to detect failing manufacturing apparatuses, early detection of failing manufacturing apparatuses becomes difficult.

Briefly recapitulating, the Applicant's invention is directed to a system, a method, and a computer program product for detecting failure of manufacturing apparatuses, capable of appropriately extracting yield data while taking account of the time axis to understand the situation, thus enhancing detection sensitivity.

Claim 1 of the present application recites a system for detecting failure of manufacturing apparatuses comprising, among other features, a low-yield detecting portion which identifies a low-yield-period apparatus having a significantly lower yield period compared with other manufacturing apparatus and the significantly lower yield period by comparing yields of a plurality of manufacturing apparatuses used in parallel in a specific manufacturing process for each time period when the manufacturing apparatuses were used, a

downward-tendency detecting portion, a warning issuing portion, and a yield data storing portion. Claim 9 recites a method of detecting failure of manufacturing apparatuses comprising, among other features, identifying a low-yield-period apparatus having a significantly lower yield period compared with other manufacturing apparatus and the significantly lower yield period by comparing yields of a plurality of manufacturing apparatuses used in parallel in a specific manufacturing process for each time period when the manufacturing apparatuses were used, identifying a downward-tendency apparatus, and issuing multi-level warnings. Claim 15 recites a computer program product for detecting failure of manufacturing apparatuses comprising, among other features, an instruction configured to identify a low-yield-period apparatus having a significantly lower yield period compared with other manufacturing apparatus and the significantly lower yield period by comparing yields of a plurality of manufacturing apparatuses used in parallel in a specific manufacturing process for each time period when the manufacturing apparatuses were used, an instruction configured to identify a downward-tendency apparatus, and an instruction configured to issue multi-level warnings. The Applicant submits that the cited references, either when taken singularly or in combination, fail to disclose all of the above limitations.

According to the present invention, by appropriately extracting yield data while taking account of the time axis to understand the situation, detection sensitivity can be enhanced, and the false reporting rate can be reduced. Furthermore, countermeasures can be quickly prioritized in terms of effectiveness.

Turning now to the Morioka et al. reference, there is no disclosure of the claimed low-yield detecting portion.

The Morioka et al. reference describes an invention relating to the inspection of foreign matters or particles in a mass production line of a semiconductor fabrication process. The Morioka et al. reference indicates that the number of foreign particles does not increase gradually but rather increases quite suddenly, so that the generation of the foreign particles must be detected as soon as possible, otherwise the number of defects becomes greater and the yield becomes lower (column 4, lines 26-53). Furthermore, since the monitors of foreign particles can make sampling on a real time basis, they can prevent in advance mass defects that would otherwise be very critical to the yield, and can provide the effect of stably securing the yield (column 12, lines 50-58). In Figure 21, the Morioka et al. reference depicts a foreign particle detecting optical system by a wafer comparison inspection. A comparison circuit (1463) compares the memory image of the first product wafer and a second memory image of the second product wafer; thereby the system can actualize the existence of any foreign particles.

On the other hand, in the present invention, the low-yield detecting portion compares “yields” of a plurality of manufacturing apparatuses used in parallel in a specific manufacturing process for each time period when the manufacturing apparatuses were used. So, the present invention clearly uses yields that are not utilized on a real time basis, but rather used by collecting yields and later comparing that information. Further, the Morioka et al. reference does not disclose a comparison of yields of *manufacturing apparatuses used in*

parallel in a specific manufacturing process, or a comparison of yields of such apparatuses for each time period when the manufacturing apparatuses were used.

Thus, the Applicant submits that the Morioka et al. reference does not disclose a low-yield detecting portion which identifies a low-yield-period apparatus having a significantly lower yield period compared with other manufacturing apparatus and the significantly lower yield period by comparing yields of a plurality of manufacturing apparatuses used in parallel in a specific manufacturing process for each time period when the manufacturing apparatuses were used, as recited in the claims. Thus, the invention of the Morioka et al. reference differs substantially from the claimed invention and cannot achieve the effectiveness of the claimed invention described above.

Furthermore, the Applicant submits that the Chen et al. reference does not supplement the deficiencies in the teachings of the Morioka et al. reference discussed above. More specifically, the Chen et al. reference does not disclose a low-yield detecting portion which identifies a low-yield-period apparatus having a significantly lower yield period compared with other manufacturing apparatus and the significantly lower yield period by comparing yields of a plurality of manufacturing apparatuses used in parallel in a specific manufacturing process for each time period when the manufacturing apparatuses were used, as recited in the claims.

The Chen et al. reference describes a system for determining whether unusual numbers of failures are occurring at final wafer sort testing, and if so, whether these failures are due to test procedure errors, or test equipment problems, or statistical quirks, or

manufacturing defects. The Chen et al. reference describes several different testing procedures, such as testing the performance of an individual operator (column 26, lines 56-67), the performance of a piece of equipment at a given physical location (column 27, lines 1-15), trends of pieces of equipment (column 27, lines 52-61), etc. However, the Chen et al. reference does not disclose comparing yields of a plurality of manufacturing apparatuses used in parallel in a specific manufacturing process as a way of identifying a low-yield-period apparatus. The invention of the Chen et al. reference does not recognize the problems discussed above with respect to the related art, and does not provide an apparatus that overcomes these problems.

The Applicant respectfully submits that the rejection is based on the improper application of hindsight considerations. It is well settled that it is impermissible simply to engage in hindsight reconstruction of the claimed invention, using Applicant's structure as a template and selecting elements from the references to fill in the gaps. *In re Gorman*, 933 F.2d 982, 18 USPQ2d 1885 (Fed. Cir. 1991). Recognizing, after the fact, that a modification of the prior art would provide an improvement or advantage, without suggestion thereof by the prior art, rather than dictating a conclusion of obviousness, is an indication of improper application of hindsight considerations. Simplicity and hindsight are not proper criteria for resolving obviousness. *In re Warner*, 397 F.2d 1011, 154 USPQ 173 (CCPA 1967).

Accordingly, the Applicant respectfully requests the withdrawal of the obviousness rejection of Claims 1, 9 and 15.

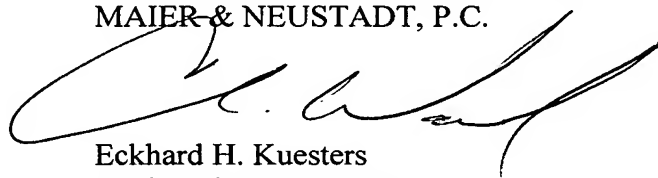
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The dependent claims are considered allowable for at least the reasons advanced for the independent claims from which they depend.

Consequently, in view of the above discussion, it is respectfully submitted that the present application is in condition for formal allowance and an early and favorable reconsideration of this application is therefore requested.

Respectfully Submitted,

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